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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,274	06/27/2003	Satoshi Seo	60188-566	4710

7590 07/25/2006

EXAMINER
NGUYEN, KHIEM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/25/2006

Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,274	SEO ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6,7 and 14* is/are allowed.

6)☒ Claim(s) *1-5,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 15th, 2006 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-7 and 13-15) are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

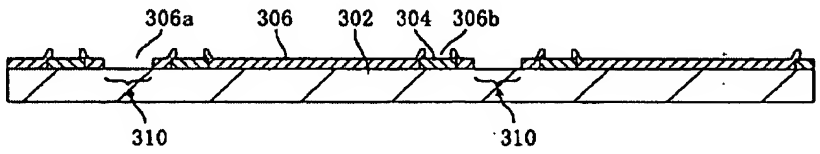
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Farnworth et al. (U.S. Patent 6,097,087).

In re claim 1, **AAPA** discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and FIGS. 20A-22):

(a) forming bonding pads **304** above a wafer **302** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (Background of the Invention, page 1, lines 10-16 and FIG. 20A);

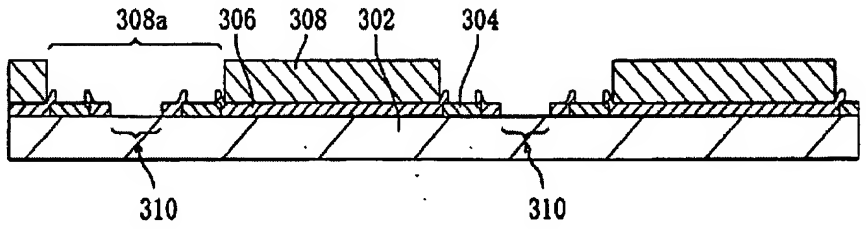
FIG. 20A
PRIOR ART



(b) forming a passivation film **306** having apertures **306a and 306b** including regions of the passivation film **306** located above parts of the bonding pads **304** and scribe line regions **310** after the step (a) (Background of the Invention, page 1, lines 16-21 and FIG. 20A);

(c) forming a buffer coat film **308** for covering part of the passivation film **306** after the step (b), and removing a region of the buffer coat film extending from an edge of the wafer and located on the whole periphery region having a certain distance from the periphery of the wafer (Background of the invention, page 1, lines 22-26 and FIG. 20B);

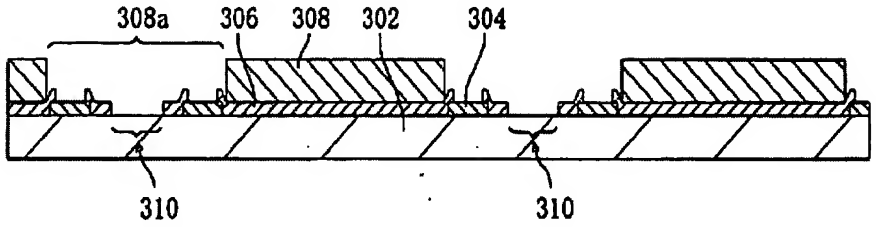
FIG. 20B
PRIOR ART



(d) forming, in the buffer coat film **308**, apertures **308a** including regions of the buffer coat film, above the scribe line regions **310** and above the parts of the bonding

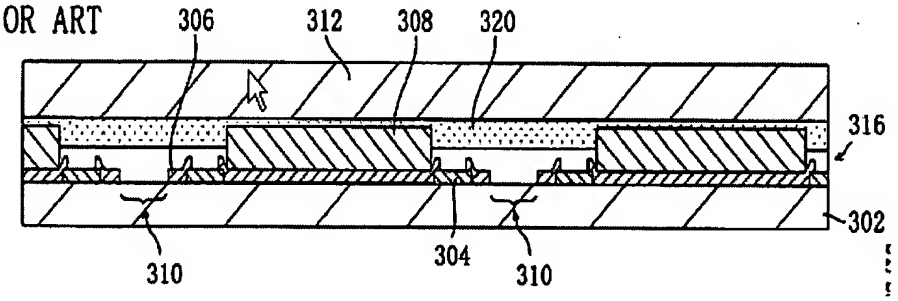
pads **304**, respectively (Background of the Invention, page 1, line 22 to page 2, line 5 and FIG. 20B);

FIG. 20B
PRIOR ART



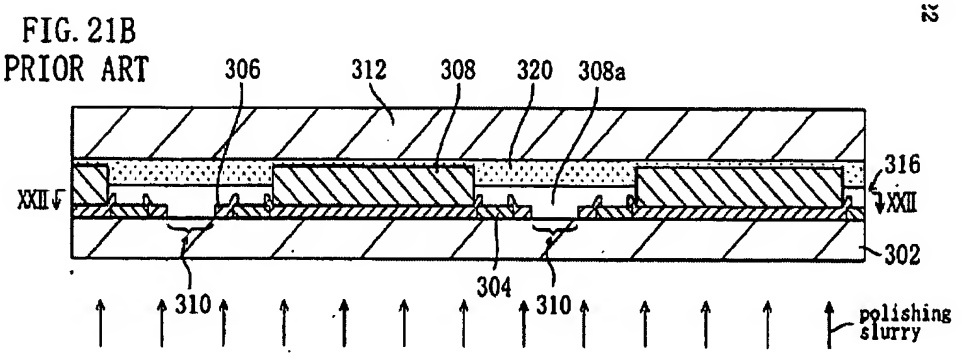
(e) bonding a surface protection tape **312** to the wafer using an adhesive material **320** after the step (d) (Background of the Invention, page 2, lines 2-5 and FIG. 21A); and

FIG. 21A
PRIOR ART



(f) polishing the rear surface of the wafer **302** after the step (e) **(polishing slurry)** (Background of the Invention, page 2, lines 6-14 and FIG. 21B).

FIG. 21B
PRIOR ART



AAPA discloses in FIG. 21B as mentioned above the step (e) of bonding a surface protection tape **312** to the wafer **302** using an adhesive material **320** and polishing the rear surface of the wafer after the step (e) but does not explicitly disclose that the bonding step including an adhesive material which contacts the passivation film in the whole periphery region of the wafer after the step (d).

Farnworth, however, discloses a process of bonding a surface protection tape **36** to the wafer **32** using an adhesive material **52** which contacts the passivation film **50** in the whole periphery region of the wafer **32** (col. 5, line 53 to col. 6, line 23 and FIG. 4).

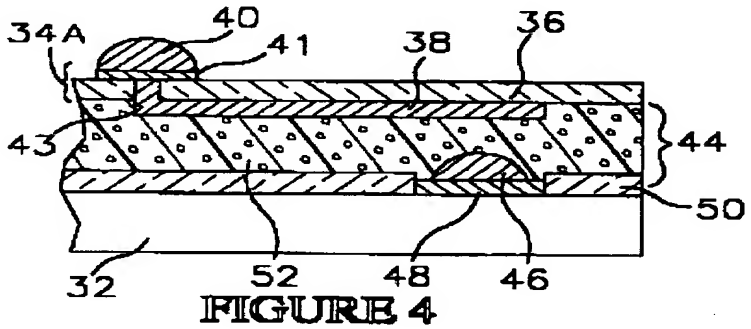


FIGURE 4

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of AAPA and Farnworth to enable the protection tape bonding process of AAPA to be performed and furthermore to provide separate electrical paths between the solder bumps and flex circuit conductors (col. 6, lines 1-2, Farnworth).

In re claim 2, as applied to claim 1 above, **AAPA** discloses that in the step (c), the buffer coat film **308** is formed using a positive-type photosensitive material, and the step (d) includes a process for exposing part of the buffer coat film **308** located on the

periphery region of the wafer **302** (Background of the Invention, page 1, lines 22-26 and FIGS. 20A-21B).

In re claim 3, as applied to claim 1 above, **AAPA** discloses that in the step (c), the buffer coat film **308** is formed using a positive-type photosensitive material, and the step (d) includes a process for exposing part of the buffer coat film **308** located on the wholes of chip regions (not shown) at least partly overlapped with the periphery region of the wafer **302** (Background of the Invention, page 1, lines 22-26 and FIGS. 20A-21B).

In re claim 4, as applied to claim 1 above, **AAPA** discloses that in the step (c), the buffer coat film **308** is formed using an organic resin, and the step (d) includes a process for selectively removing part of the buffer coat film 308 located on the periphery region of the wafer **302** by a solvent (AAPA, page 1, lines 22-26).

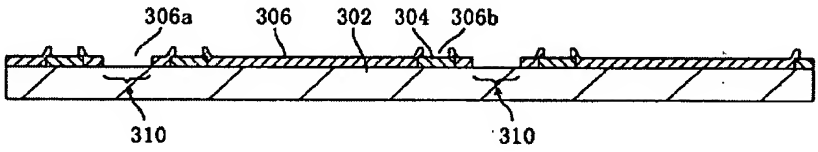
In re claim 5, as applied to claim 1 above, **AAPA** discloses that in the step (c), the buffer coat film **308** is formed using an organic resin, and the step (d) includes a process for blowing gas on part of the buffer coat film **308** located on the periphery region of the wafer **302** before the curing of the buffer coat film (AAPA, page 1, lines 22-24 and FIGS. 21A-B).

In re claim 13, as applied to claim 1 above, **AAPA** discloses that in the step (d), the whole peripheral region refers to circular regions in the periphery of the wafer **302** (FIGS. 20A-21B and related text).

In re claim 15, **AAPA** discloses a method for fabricating a semiconductor device, the method comprising the steps of (Background of the invention, pages 1-2 and FIGS. 20A-22):

(a) forming bonding pads **304** above a wafer **302** on which semiconductor elements (not shown) and an interconnect layer (not shown) are formed (Background of the Invention, page 1, lines 10-16 and FIG. 20A);

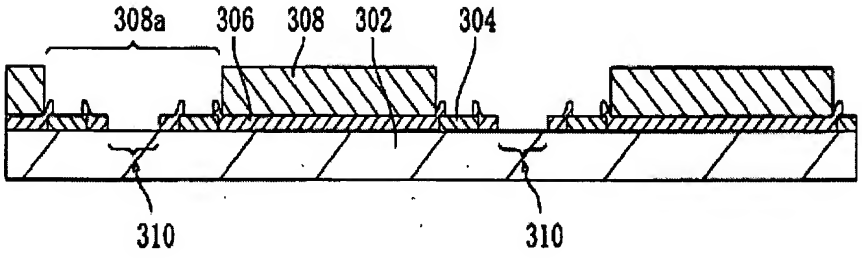
FIG. 20A
PRIOR ART



(b) forming a passivation film **306** having apertures **306a and 306b** including regions of the passivation film **306** located above parts of the bonding pads **304** after the step (a) (Background of the Invention, page 1, lines 16-21 and FIG. 20A);

(c) forming a buffer coat film **308** for covering part of the passivation film **306** after the step (b) (Background of the invention, page 1, lines 22-26 and FIG. 20B);

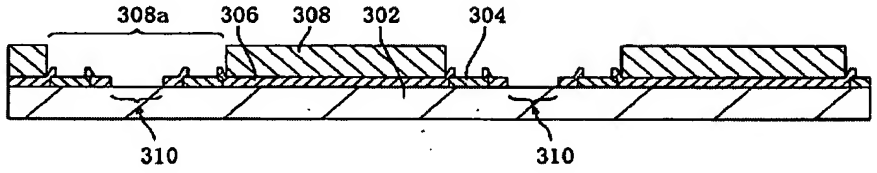
FIG. 20B
PRIOR ART



(d) forming, in the buffer coat film **308**, apertures **308a** including regions of the buffer coat film **308** located above a periphery region having a certain distance from the peripheral of the wafer **302**, above the scribe line regions **310** and above the parts of the

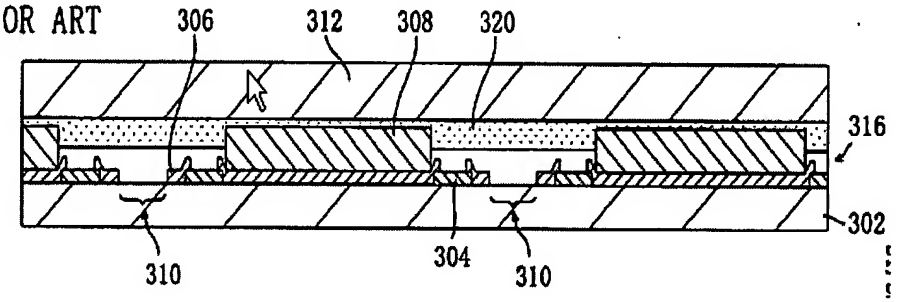
bonding pads **304**, respectively (Background of the Invention, page 1, line 22 to page 2, line 5 and FIG. 20B);

FIG. 20B
PRIOR ART



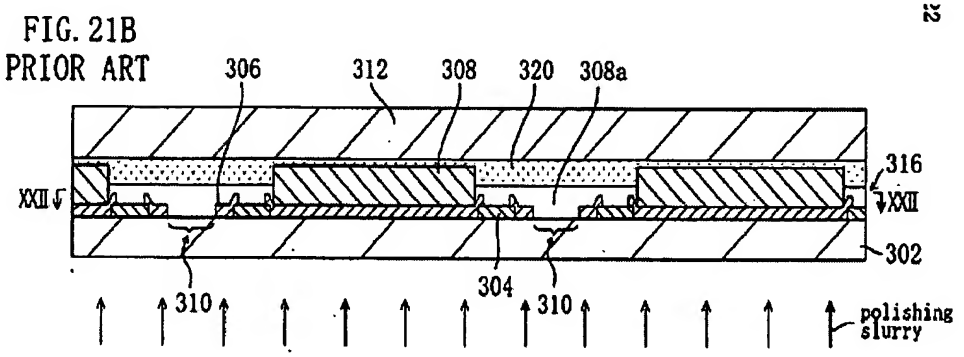
(e) bonding a surface protection tape **312** to the wafer using an adhesive material **320** after the step (d) (Background of the Invention, page 2, lines 2-5 and FIG. 21A); and

FIG. 21A
PRIOR ART



(f) polishing the rear surface of the wafer **302** after the step (e) **(polishing slurry)** (Background of the Invention, page 2, lines 6-14 and FIG. 21B).

FIG. 21B
PRIOR ART



AAPA discloses in FIG. 21B as mentioned above the step (e) of bonding a surface protection tape **312** to the wafer **302** using an adhesive material **320** and polishing the rear surface of the wafer after the step (e) but does not explicitly disclose that the bonding step including an adhesive material which contacts the passivation film in the whole periphery region of the wafer after the step (d).

Farnworth, however, discloses a process of bonding a surface protection tape **36** to the wafer **32** using an adhesive material **52** which contacts the passivation film **50** in the whole periphery region of the wafer **32** (col. 5, line 53 to col. 6, line 23 and FIG. 4).

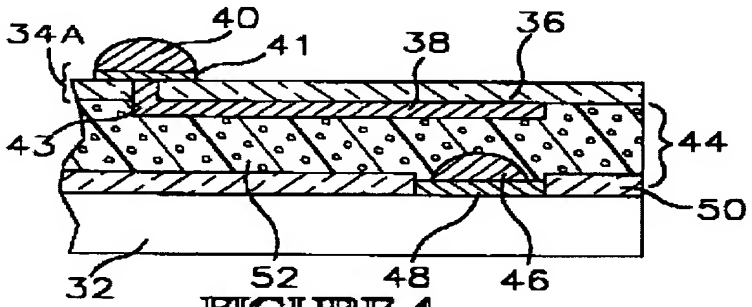


FIGURE 4

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of AAPA and Farnworth to enable the protection tape bonding process of AAPA to be performed and furthermore to provide separate electrical paths between the solder bumps and flex circuit conductors (col. 6, lines 1-2, Farnworth).

Allowable Subject Matter

4. Claims 6-7 and 14 were previously allowed as set forth in the Previous Office Action.

Response to Applicants' Amendment and Arguments

5. Applicants' arguments with respect to claims 1-5, 13, and 15 have been considered but are moot in view of the new ground(s) of rejection.

Applicants' arguments in the Amendment submitted with an RCE filed on May 15th, 2006 resulted withdrawal of the 35 U.S.C. 102(e) rejection based solely on AAPA in the Office Action mailed on February 14th, 2006. A new rejection is made as set forth in this Office Action based on AAPA and the newly discovered reference to Farnworth et al. (U.S. Patent 6,097,087) as mentioned in Paragraph 3 above.

For this reason, Examiner holds the rejection proper.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
July 20, 2006

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800